

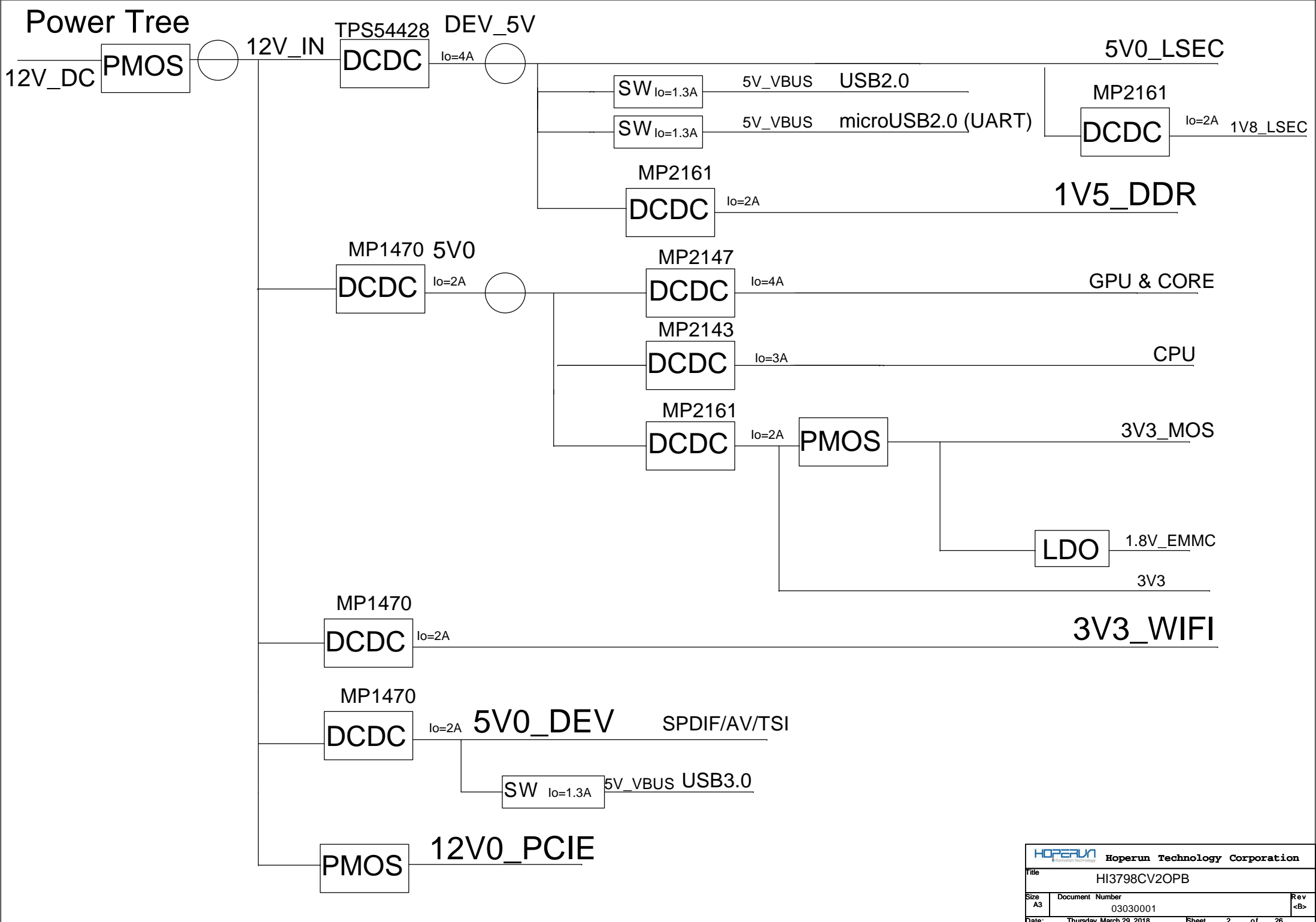
# Hi3798CV20PB VER.B

Hi3798CV200 Open Source Board  
4 layers PCB with DDR3 8bit x 4

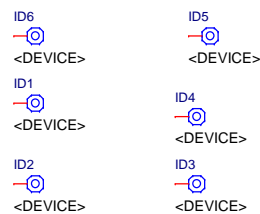
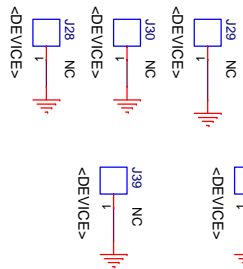
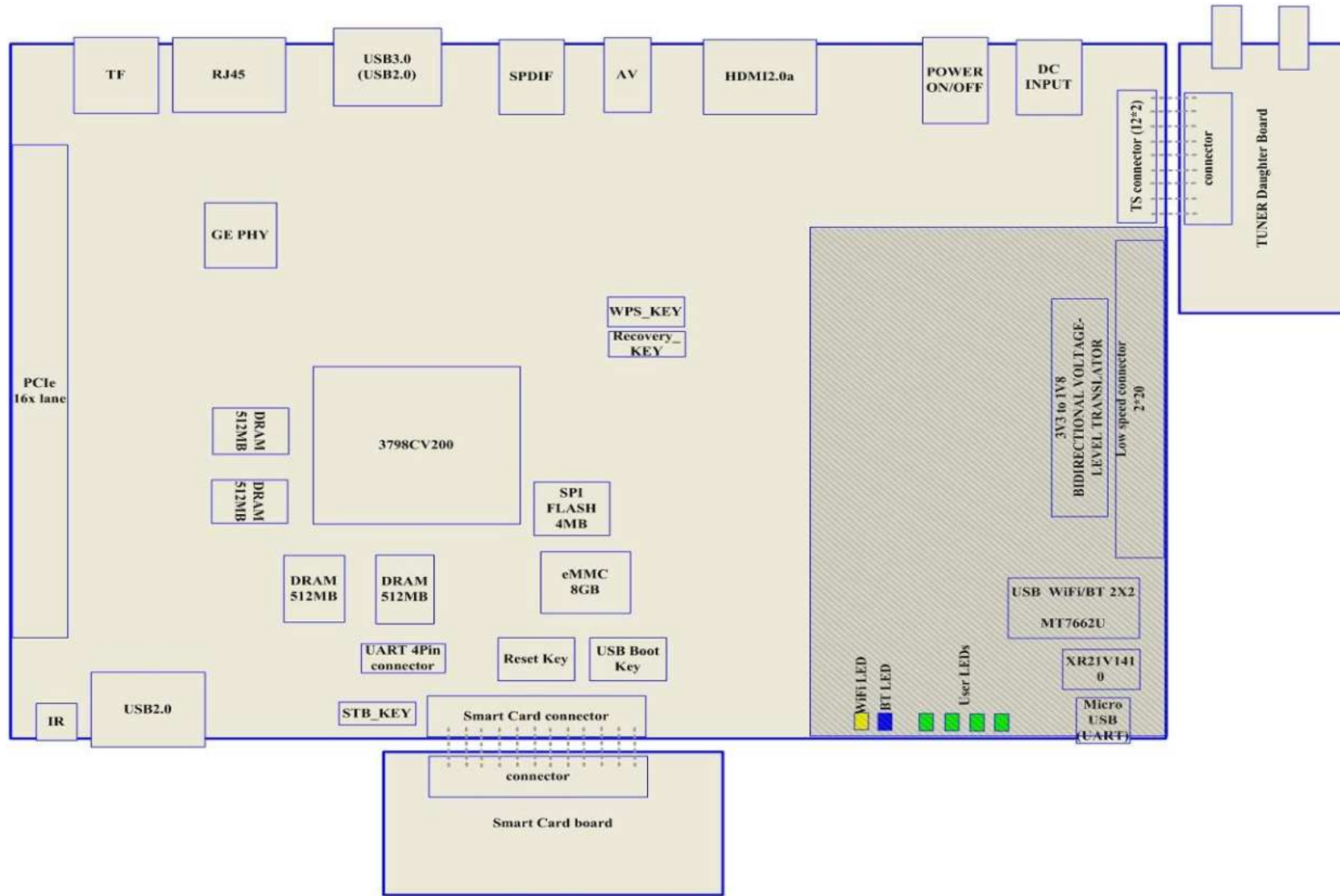
Board Size:160mm x 120mm x 1.6mm  
Hi3798CV20PB VER.B\_V1.0.0.0

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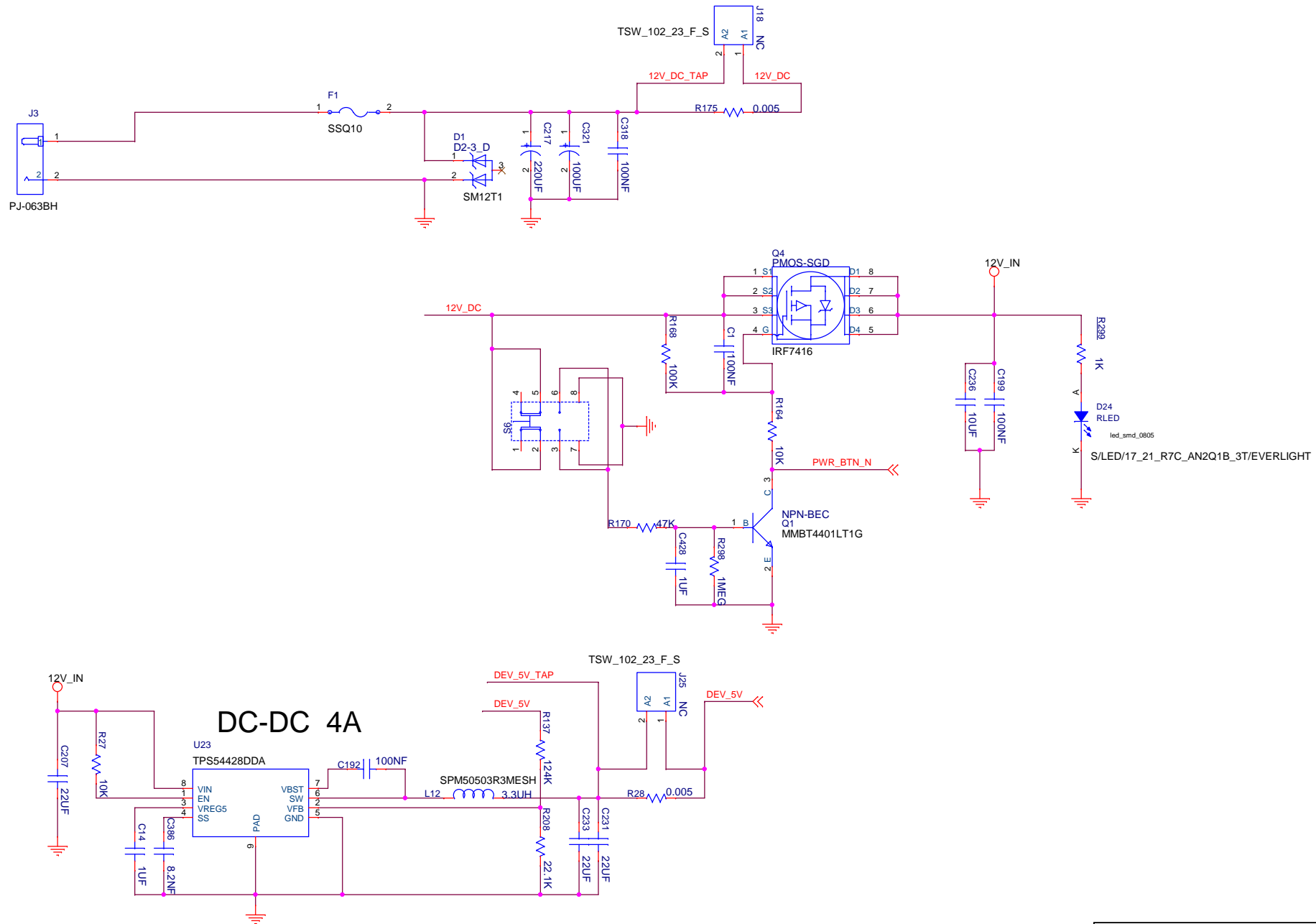
# Power Tree



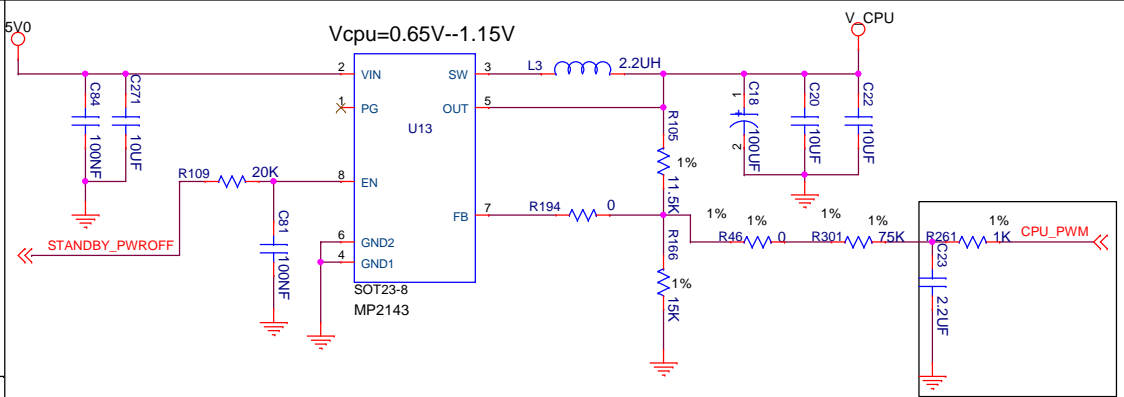
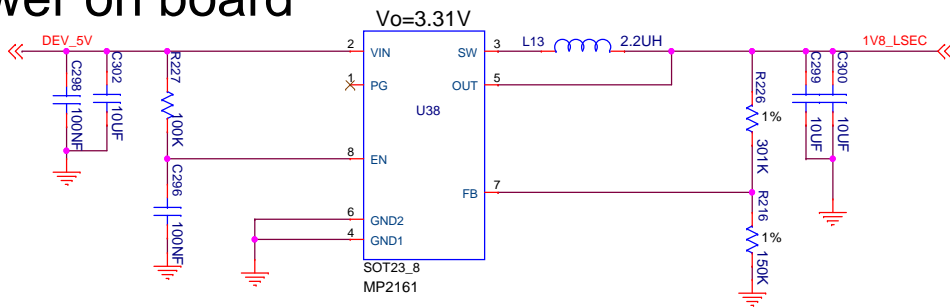
# Block Diagram



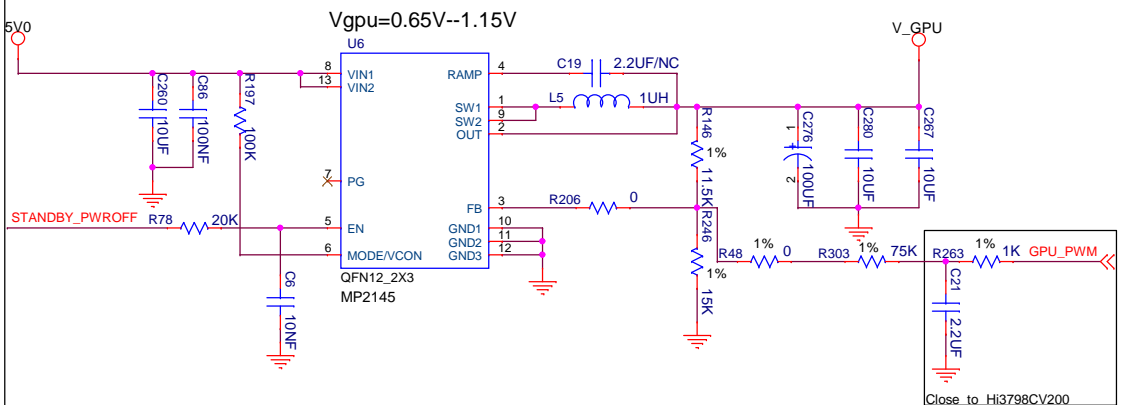
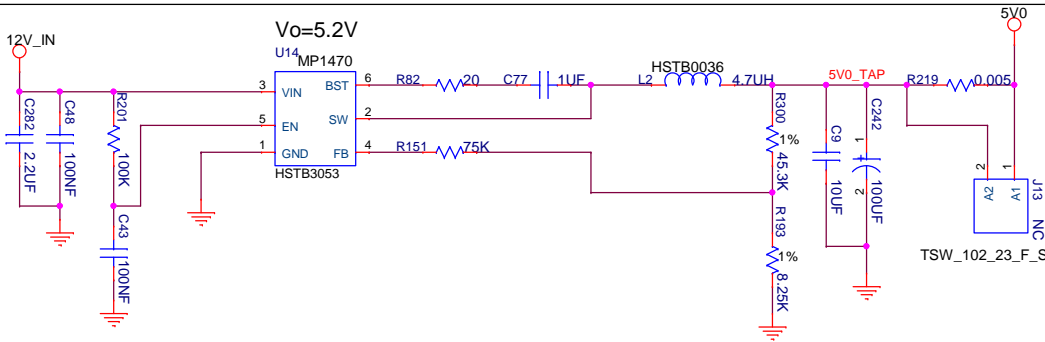
# Power on board



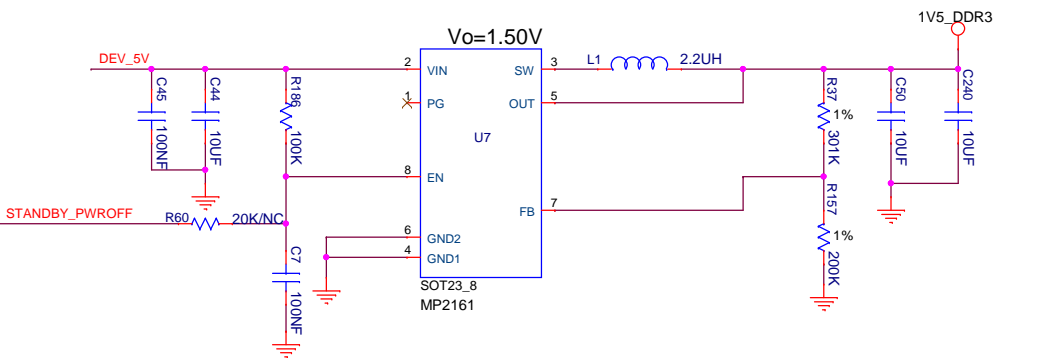
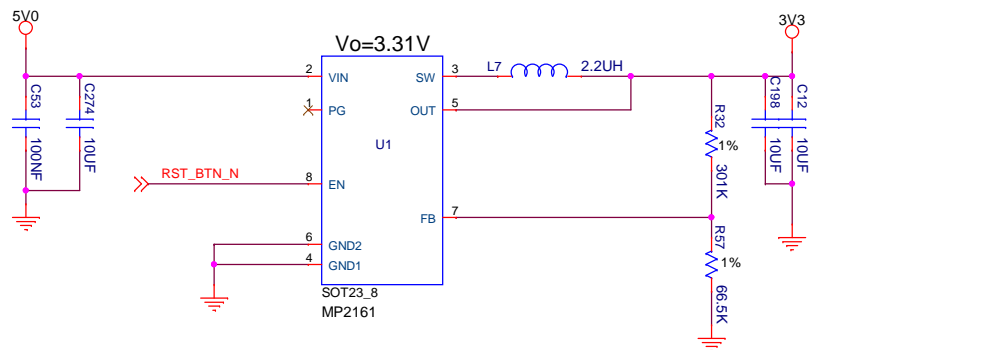
# Power on board



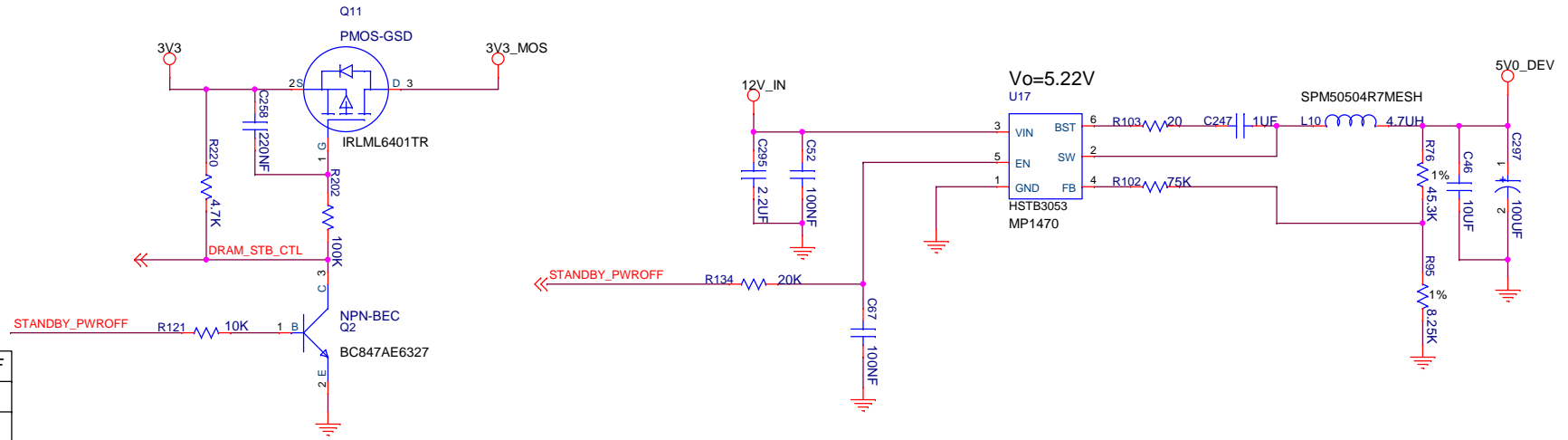
The 3A DC-DC with fast transient response(such as COT or ACOT control) must be selected for the CPU power.



The 4A DC-DC with fast transient response(such as COT or ACOT control) must be selected for the GPU power.

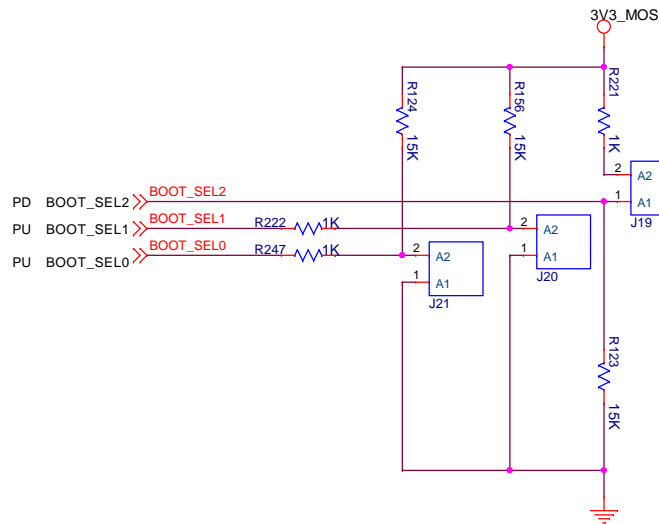


# Power Ctrl

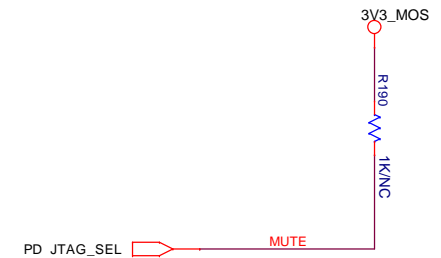


STANDBY_PWROFF	
0	Power Off
1	Power On

BOOT_SEL[2:0]	BOOT FROM
000	SPI NOR
001	NAND FLASH
010	iSD
011	eMMC(default)
100	SPI NAND
Others	Reserved



JTAG_SEL	Function
0	JTAG/TSI SEL By PIN_MUX (default)
1	JTAG



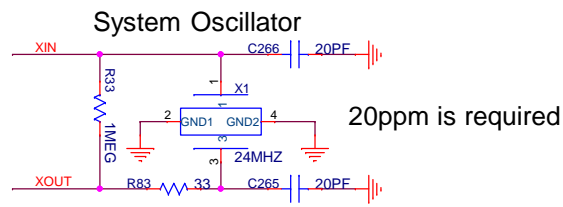
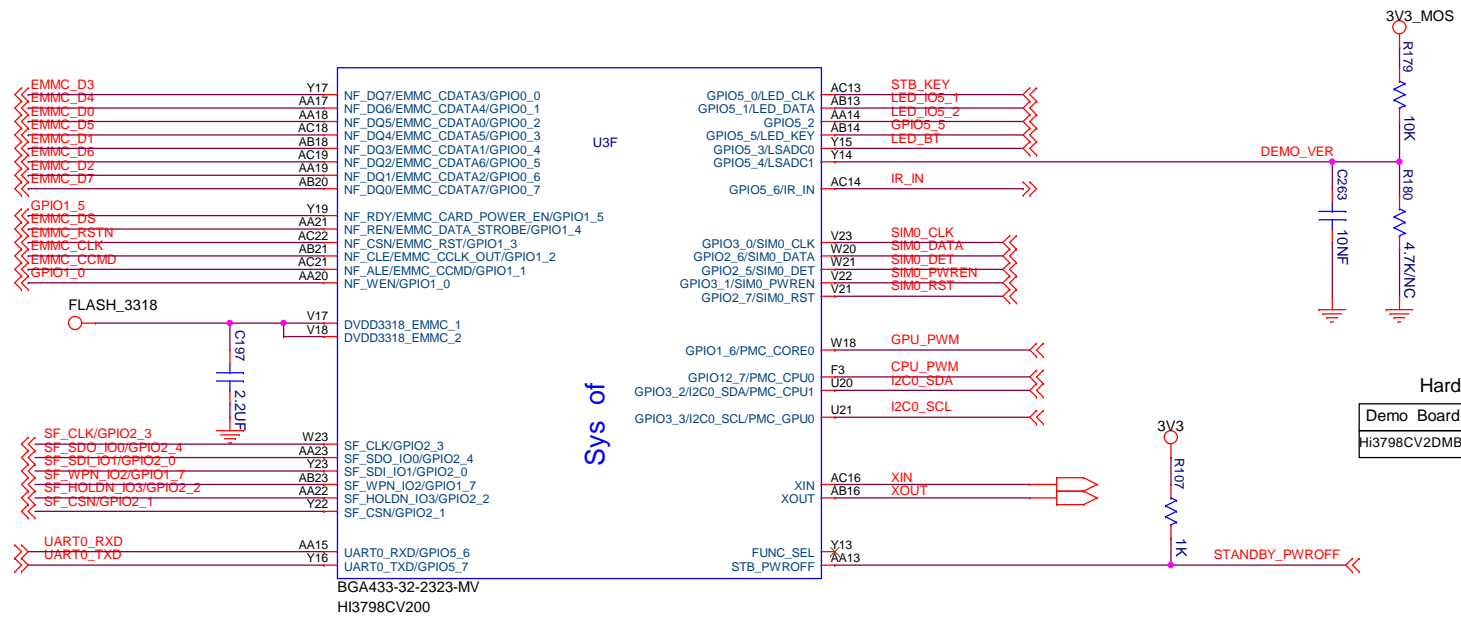
# Unit 1 of Hi3798CV200(FLASH/UART/IR/PWM/XTAL)

\*\*\*\*\*Low Speed ADC Information\*\*\*\*\*

Input Voltage Range: 0V - 3.3V( > 3.63V is forbidden)

LSADC0: used as Key input or Power detected

LSADC1: used as Hardware Version detected



# Unit 2 of Hi3798CV200(HDMI TX/VDAC/ADAC)

## \*\* HDMI Design guideline \*\*

### A.routing

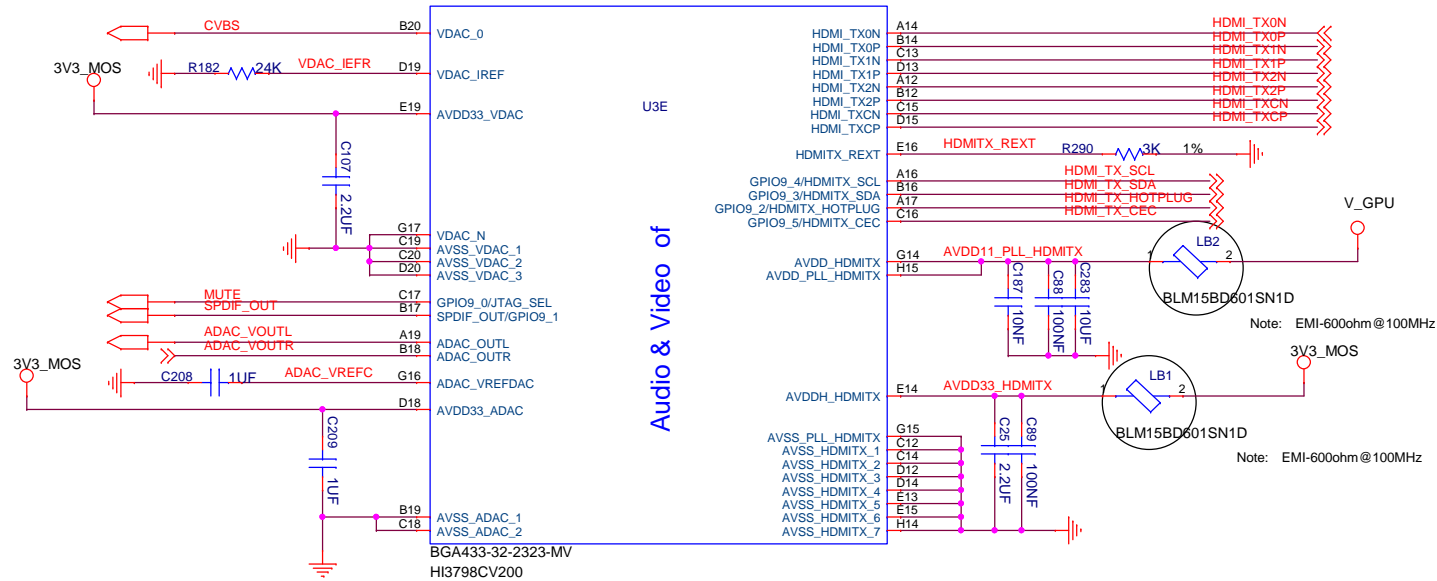
- 1.Route as 100 Ohm differential impedance.
- 2.Differential pairs should be routed on TOP layer only.

### B.trace length

- 1.The length for the differential pairs should be less than 5 inches.
- 2.Match trace length of differential pairs, 5 mils max within a pair.

### C.component selection

- 1.REXT resistor should be 3K Ohm +/-1%.
- 2.ESD components are suggested for ports protection.
- 3.All equivalent capacitance of ESD components should be < 0.35pF.



## \*\* Audio & Video Design guideline \*\*

### A.VIDEO

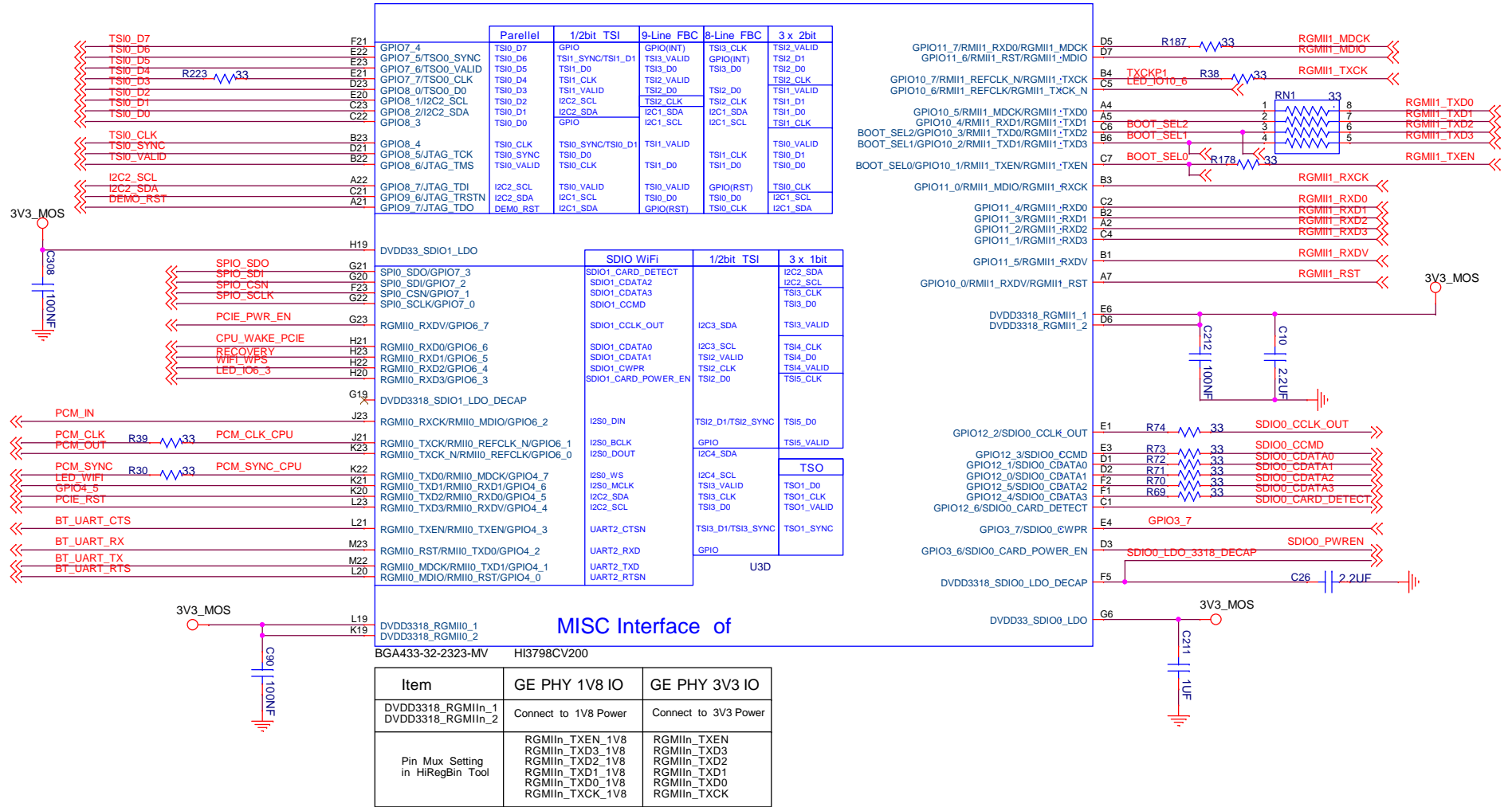
- 1.VIDEO REXT resistor should be 12K +/-1% precision for full current model, and 24K +/-1% precision for quarter current model
- 2.REXT/COMP should be traced as short as possible, and isolated from all other traces.

### B.AUDIO

- 1.VREF should be traced as short as possible, and isolated from all other traces.



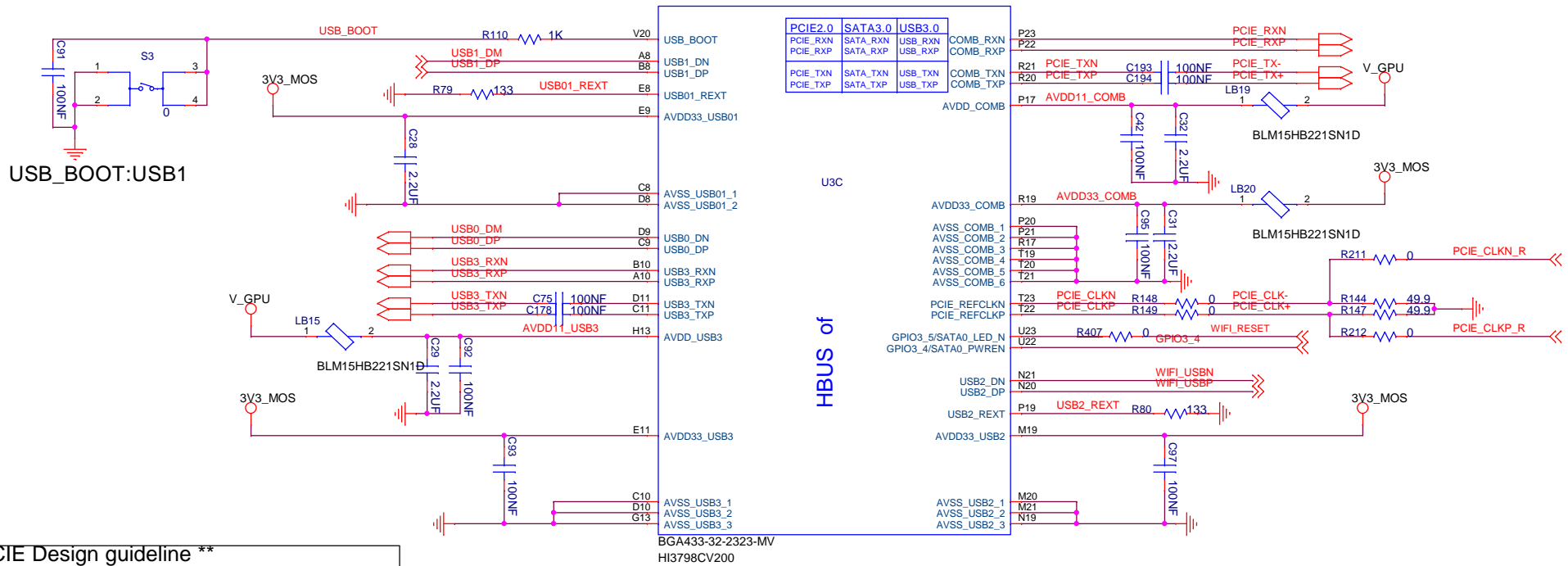
# Unit 3 of Hi3798CV200(RGMII/RMII/SDIO/TS)



## \*\*\*\*\* Design Notes \*\*\*\*\*

- DVDD33\_SDI01\_LDO is the Input of the inside LDO which is power supply for IO of SDIO1, and DVDD3318\_SDI01\_LDO\_DECAP is the decap pin of the LDO, connect 2.2uF to GND if 1V8 IOs are needed, others NC is OK.
  - DVDD3318\_RGMII0 is the power supply pin of J23/J21/K23/K22/K21/K20/L23/L21/M23/M22/L20, connect to 1V8 power if 1V8 IOs are needed, or connect to 3V3 power.
- eg1. if SDIO1 is used as SDIO3.0, DVDD33\_SDI01\_LDO should be connected to 3V3 power, DVDD3318\_SDI01\_LDO\_DECAP should be connect 2.2uF to GND.
- eg2. if RGMII0 in 1V8 IOs is used, DVDD33\_SDI01\_LDO should be connected to 3V3 power, DVDD3318\_SDI01\_LDO\_DECAP should be connect 2.2uF to GND, DVDD3318\_RGMII0 should be connect to 1V8.
- eg3. All IOs are used as 3V3 IOs, DVDD33\_SDI01\_LDO and DVDD3318\_RGMII0 should be both connected to 3V3 power, DVDD3318\_SDI01\_LDO\_DECAP needn't be care, NC is OK.

# Unit 4 of Hi3798CV200(USB2.0/USB3.0/COMBPHY(SATA/U3/PCIE))



**\*\* SATA&PCIE Design guideline \*\***

**A.routing**  
 1.Route as 100 Ohm differential impedance.  
 2.Differential pairs should be routed on TOP layer only.

**B.trace length**  
 1.The length for the differential pairs should be less than 5 inches.  
 2.Match trace length of DP and DM differential pairs, 10 mils max within a pair.

**C.component selection**  
 1.SATA:The value of capacitors for AC coupling should be  $\leq 12nF$ , default 10nF  
 2.PCIE:The value of capacitors for AC coupling should be  $\leq 200nF$ , default 100nF

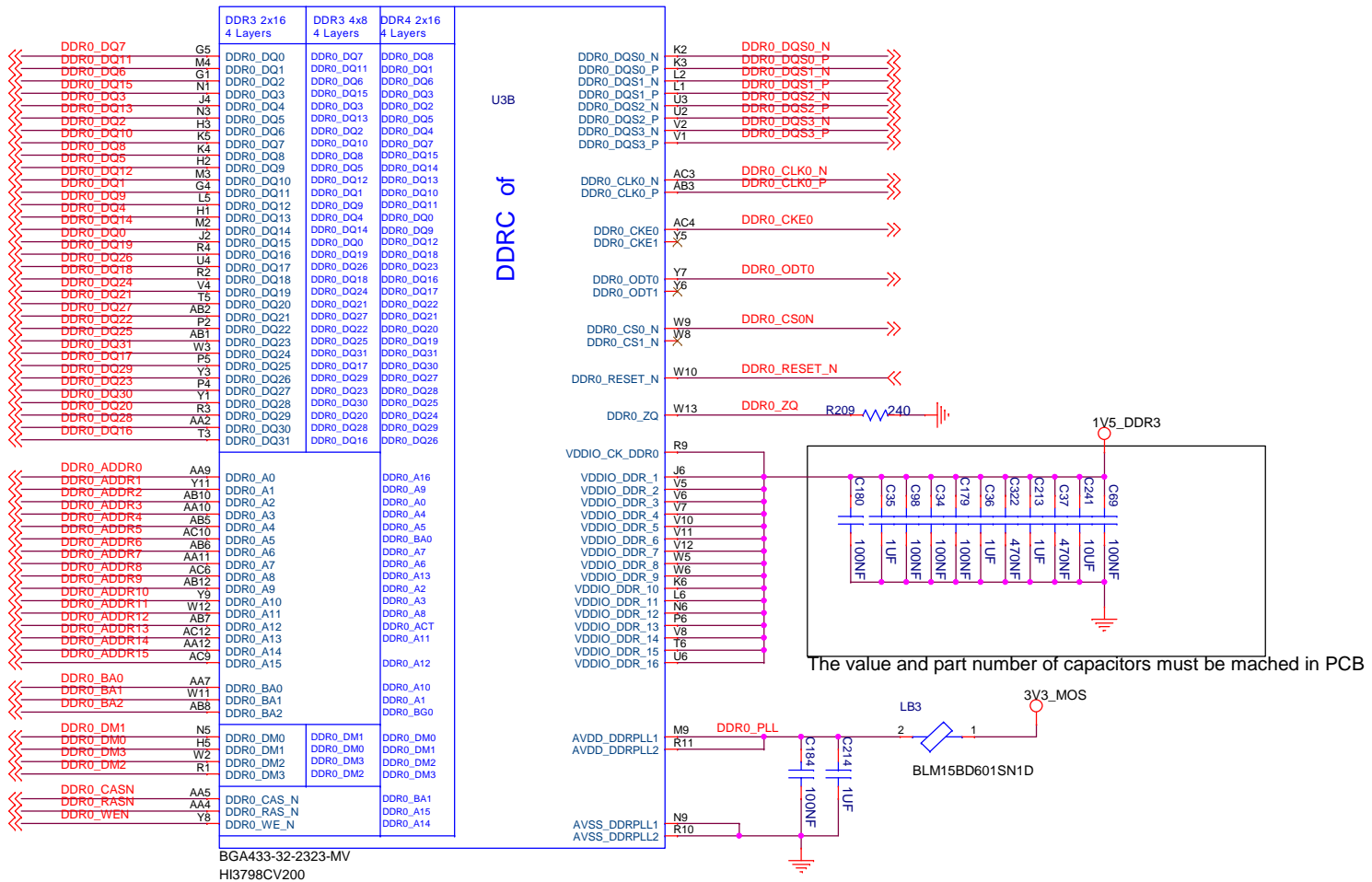
**\*\* USB Design guideline \*\***

**A.routing**  
 1.Route as 90 Ohm differential impedance.  
 2.Differential pairs should be routed on TOP layer only.

**B.trace length**  
 1.The length for the differential pairs should be less than 5 inches.  
 2.Match trace length of DP and DM differential pairs, 10 mils max within a pair.

**C.component selection**  
 1.USB2.0 REXT resistor should be 133 ohm +/-1% and USB3.0 133 ohm +/-1%  
 2.ESD components are suggested for ports protection.  
 3.Equivalent capacitance of ESD component should be  $< 1.5pF$ .

# Unit 5 of Hi3798CV200(DDRC)



## \*\* DDR Design guideline \*\*

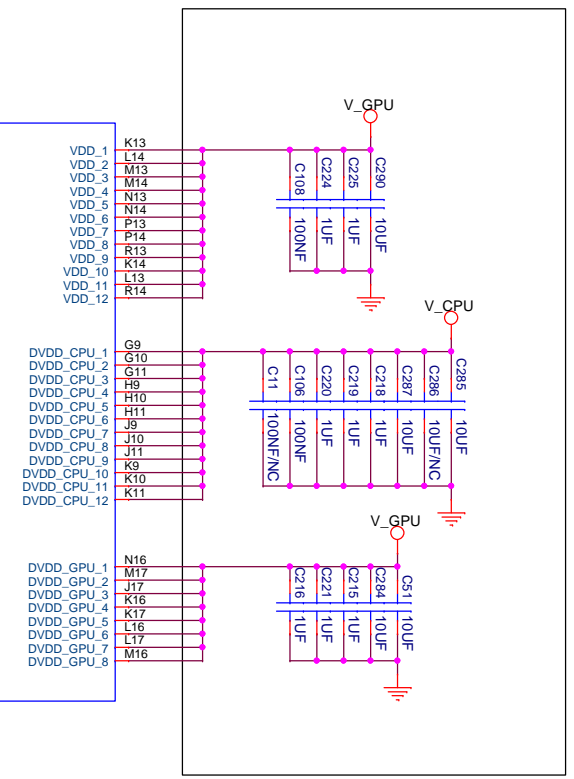
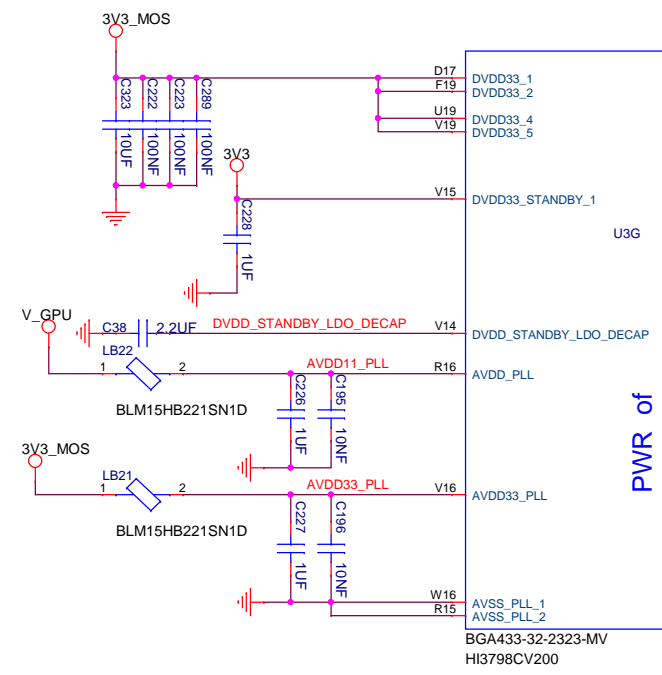
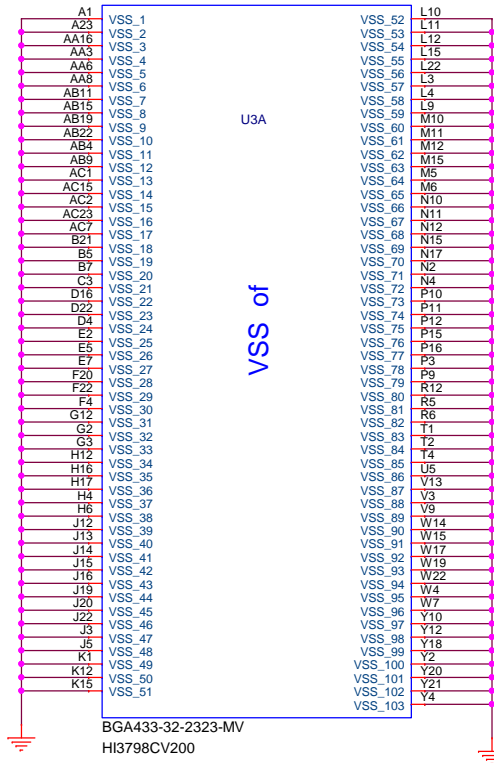
### A.general suggestion

- 1.Hi3798CV200 supports DDR3/DDR3L/DDR4
- 2.Hi3798CV200 supports up to 2GB DDR3.
- 3.The circuit of DDR\_VREF\_CA and DDR\_VREF\_DQ must be independent.
- 4.Please copy the decoupling capacitor design from hisilicon demo board.
- 5.3V3 DDRPLL is needed.

### B.Layout suggestion

1. Please copy hisilicon demo board completely

# Unit 6 of Hi3798CV200(POWER/VSS)

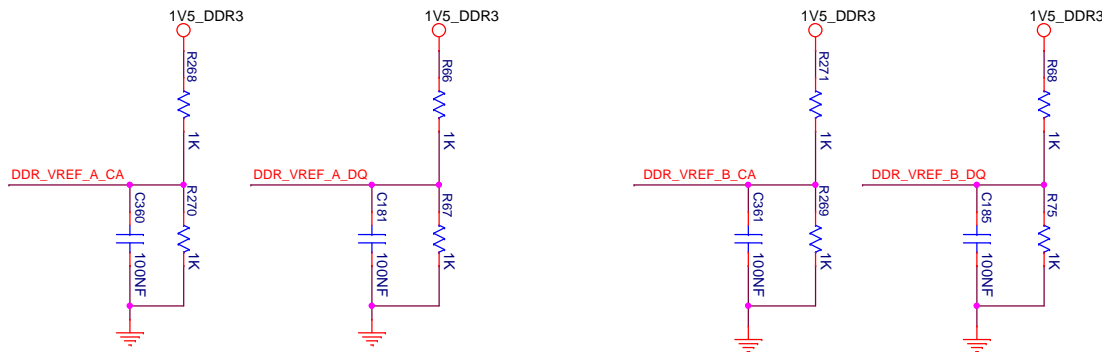
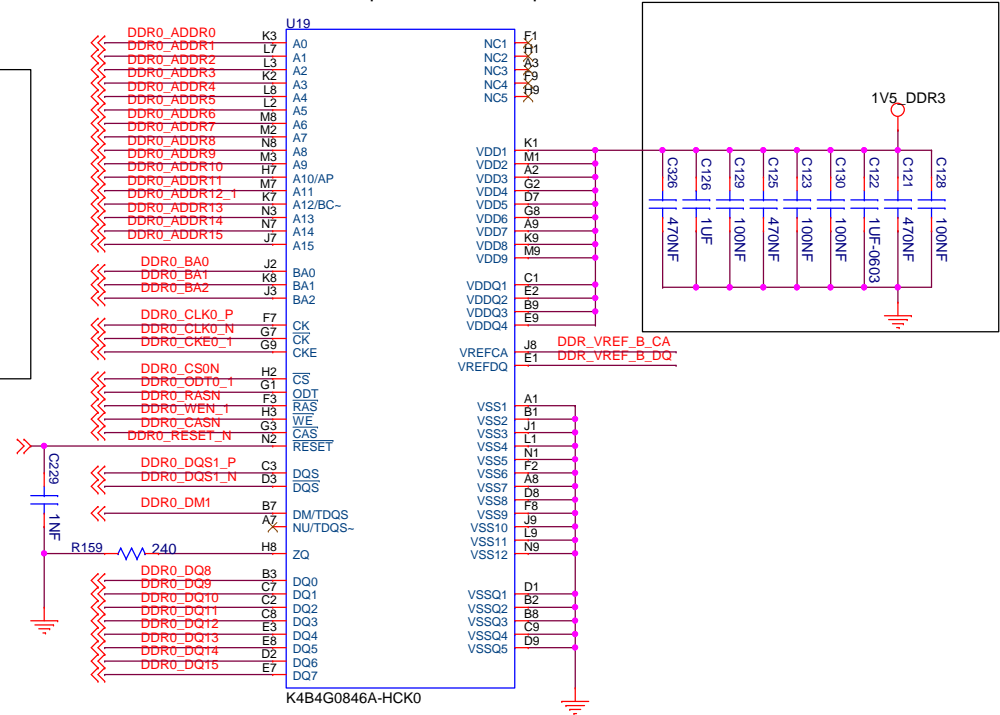
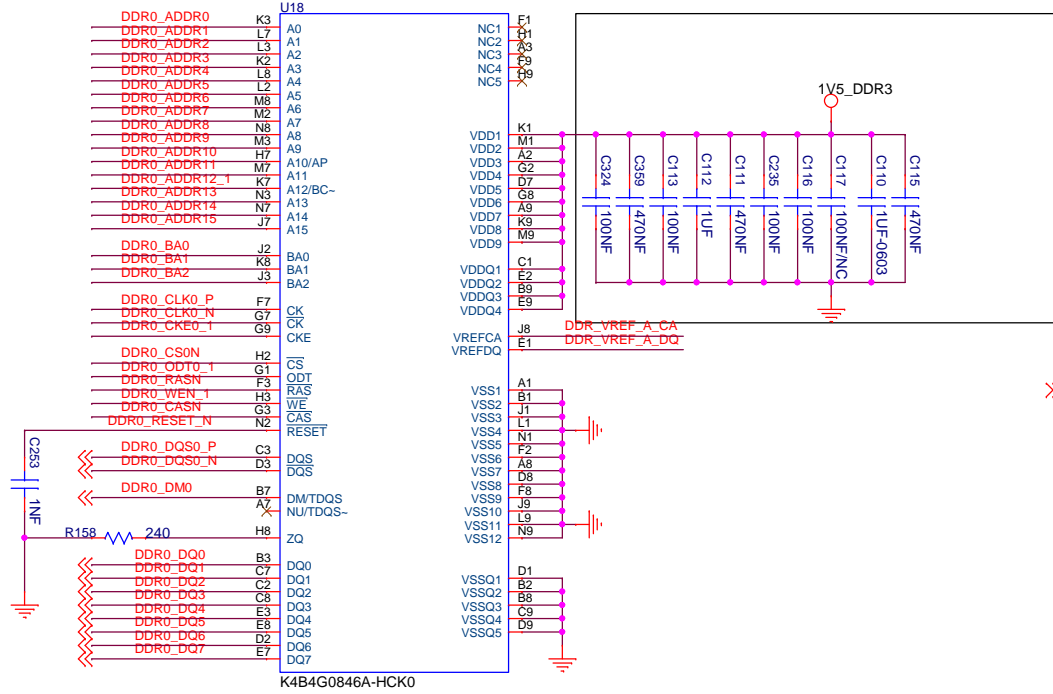


The value and part number of capacitors must be matched in PCB

# DDR Byte0 & Byte1

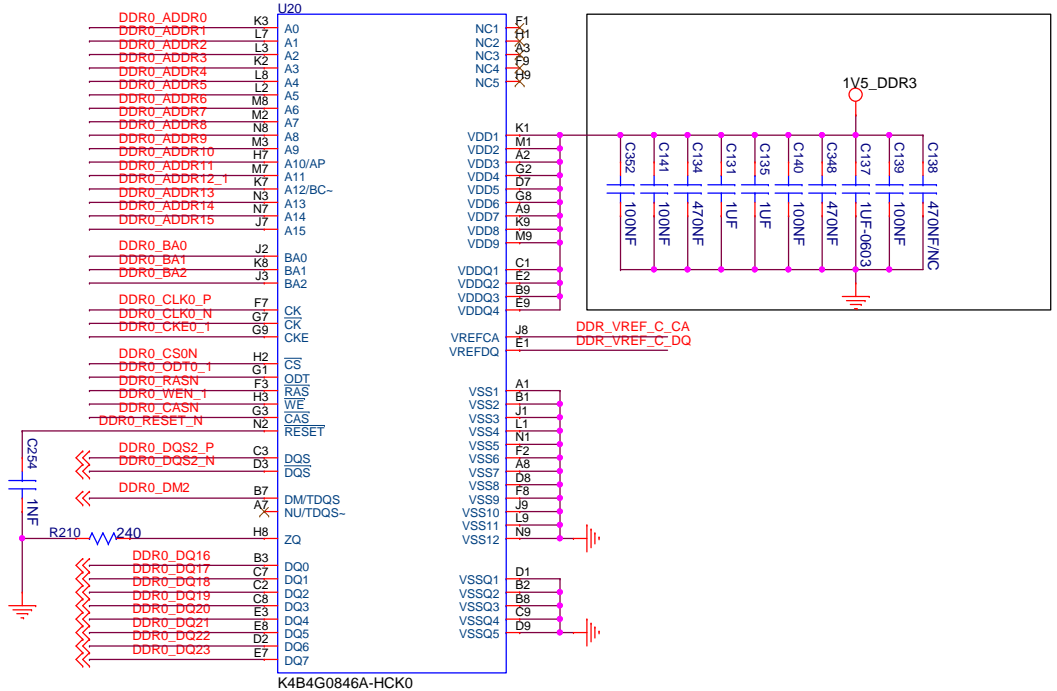
The value and part number of capacitors must be mached in PCB

The value and part number of capacitors must be mached in PCB

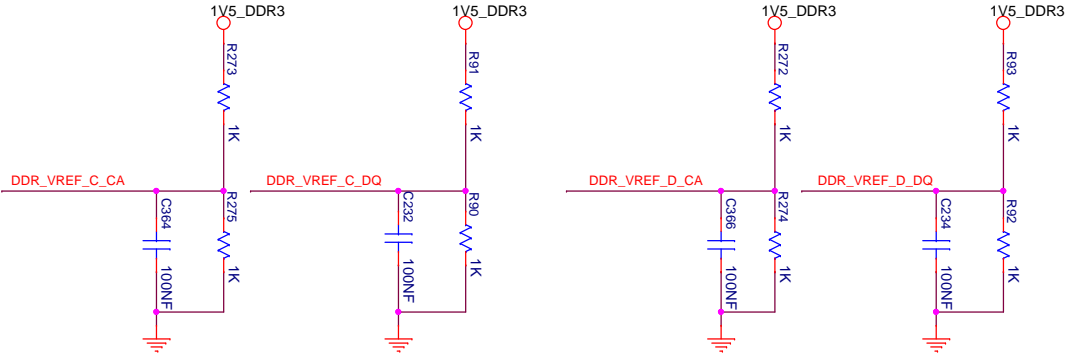
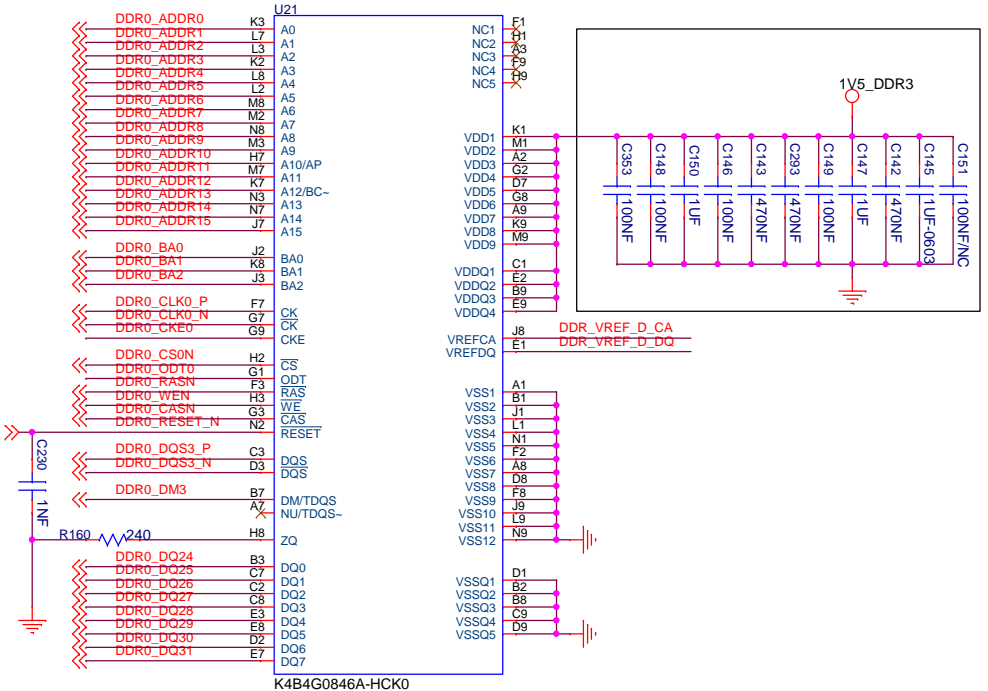


# DDR Byte2 & Byte3

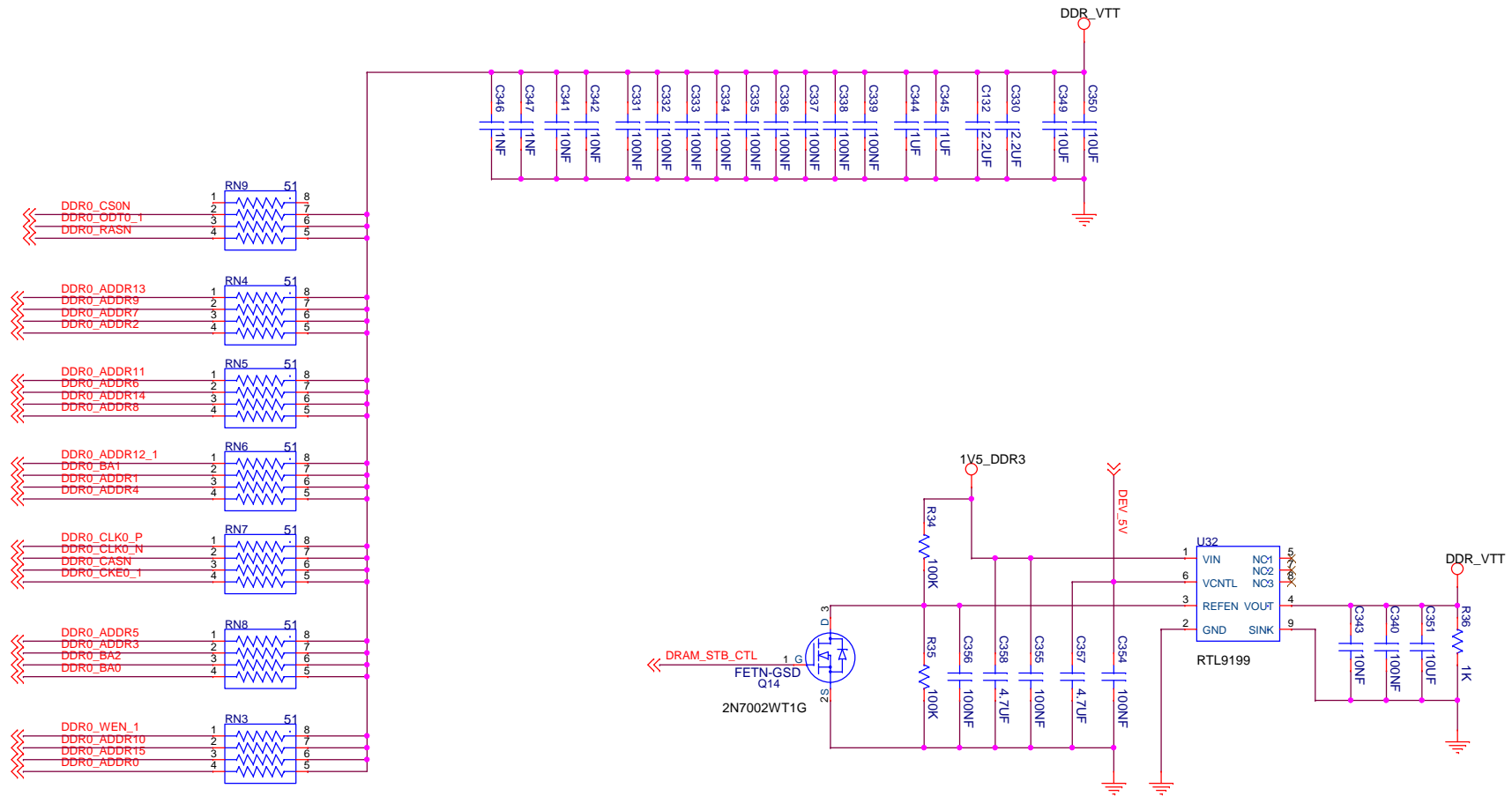
The value and part number of capacitors must be matched in PCB



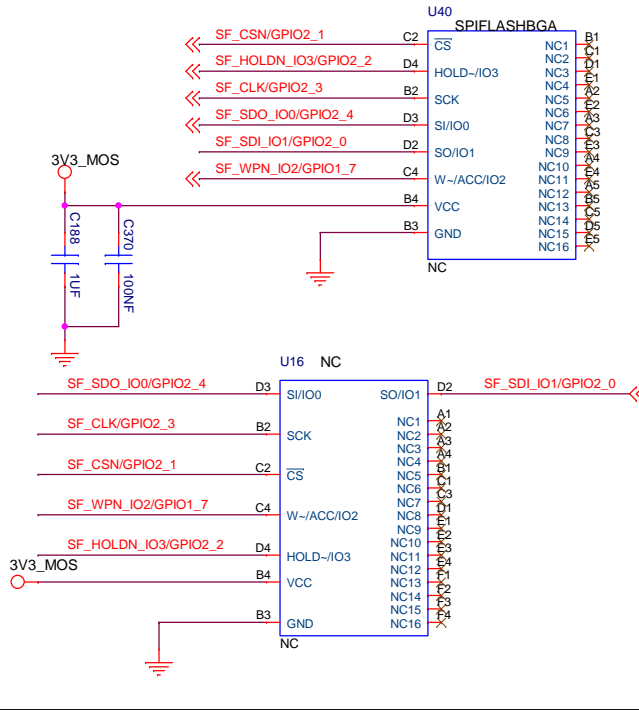
The value and part number of capacitors must be matched in PCB



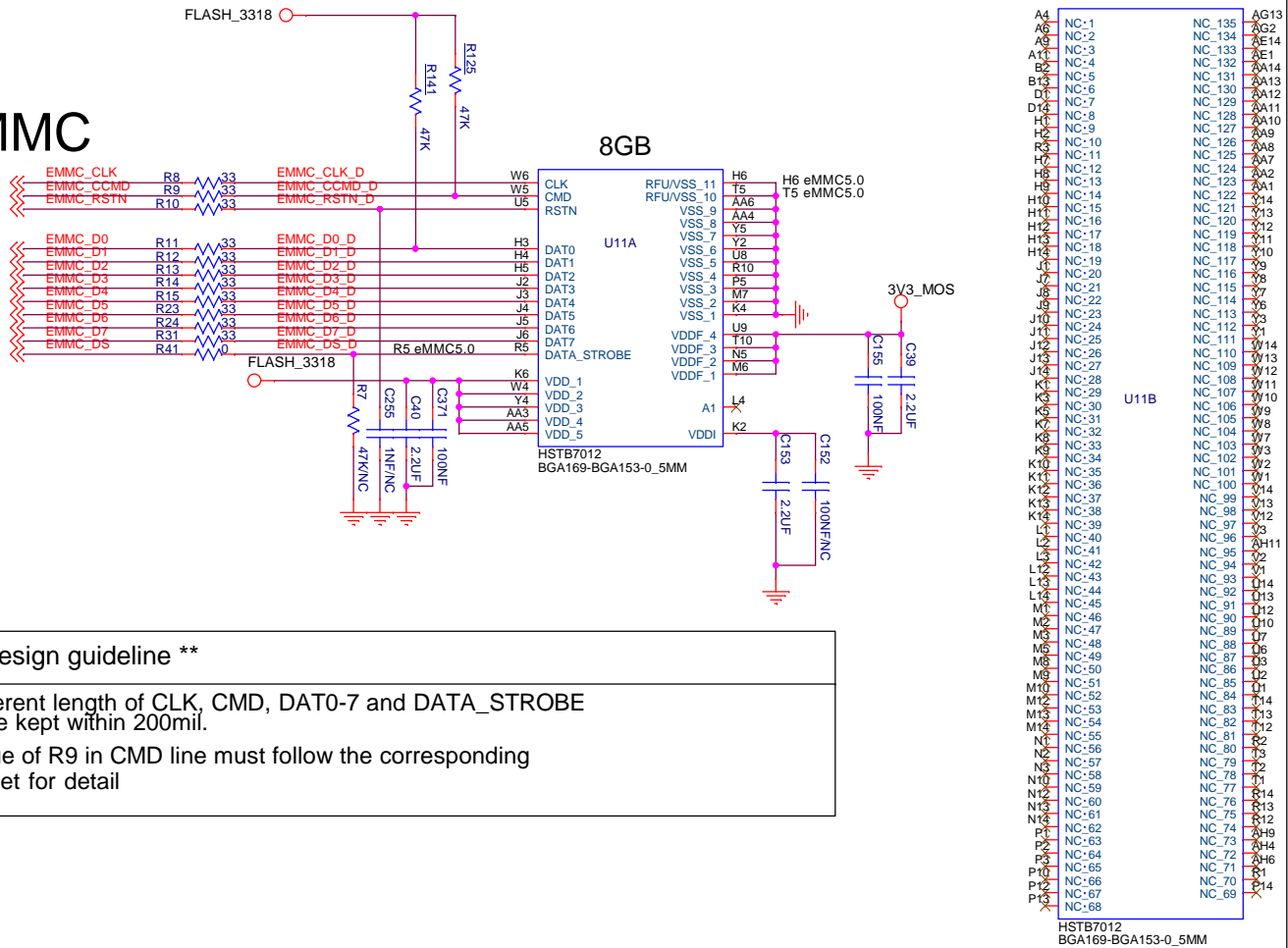
# DDR VTT



# NOR



# NOR/EMMC

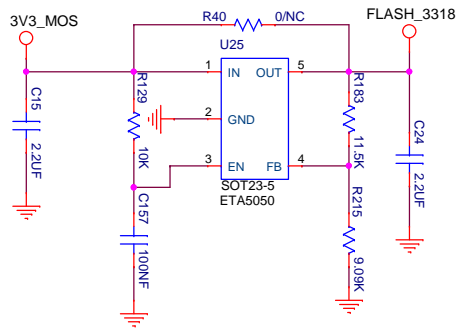


## \*\* eMMC design guideline \*\*

1. The different length of CLK, CMD, DAT0-7 and DATA\_STROBE must be kept within 200mil.
2. The value of R9 in CMD line must follow the corresponding datasheet for detail

$$VO=0.8 \times (1 + 11.5K / 9.09K) = 1.81V$$

MAX:500mA



## 3.3V IO only For eMMC DDR50 Mode

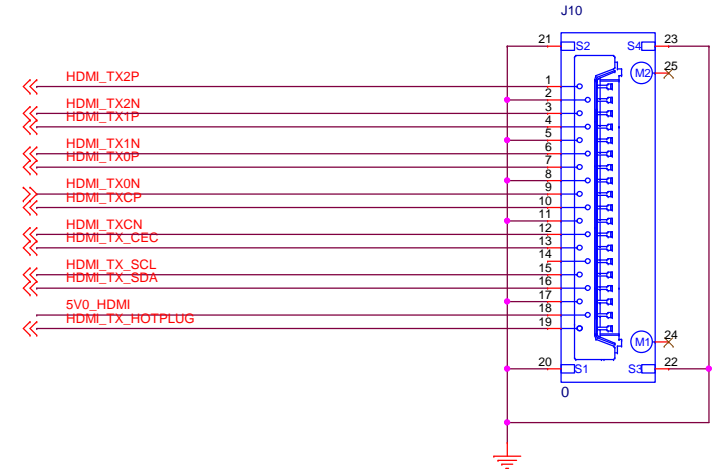
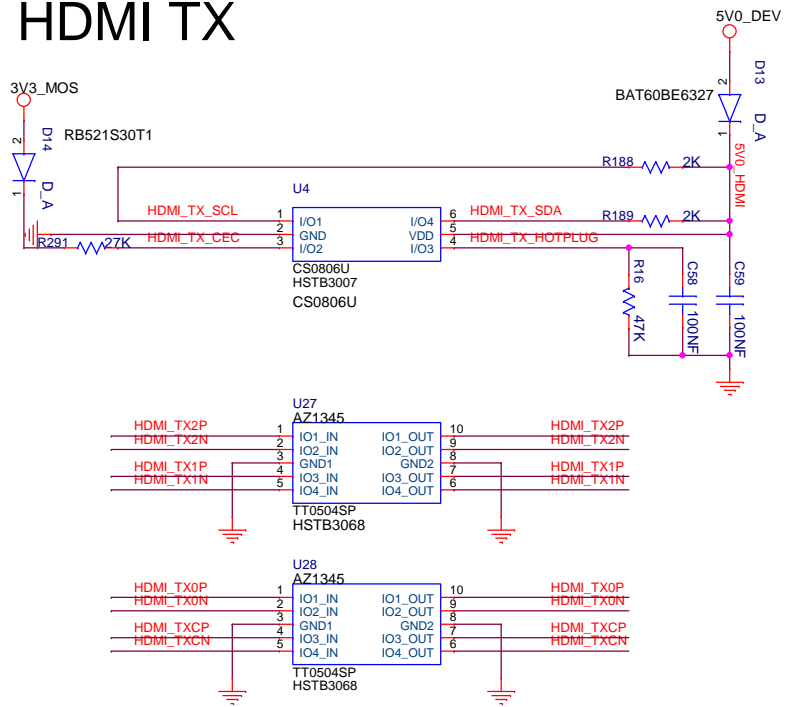
R40 = 0 ohm  
others = NC

## eMMC5.0(1.8V) default

1.8V IO For eMMC HS200\HS400 Mode  
R40 = NC  
Others Mounted

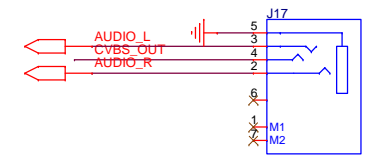
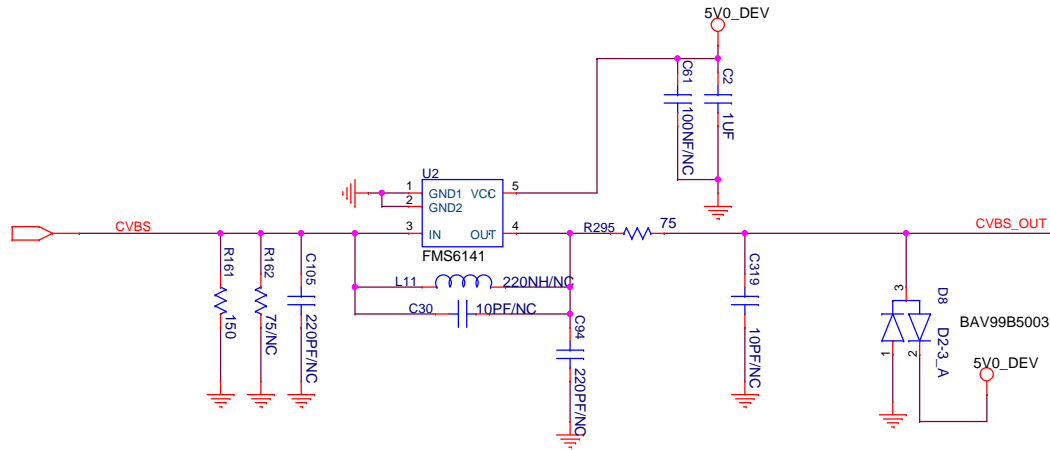


# HDMI TX



# VIDEO OUTPUT

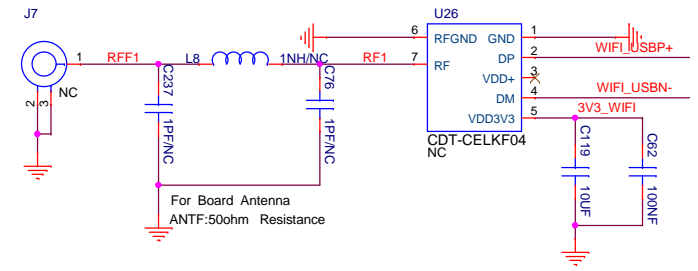
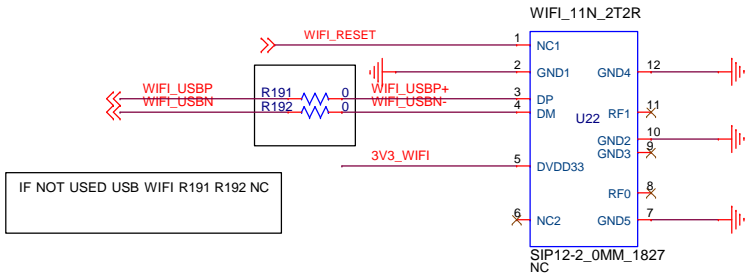
VIDEO BUFFER	LC Filter
R182 = 24K 1%	R182 = 12K 1%
R161 = 150 1%	R161 = 75 1%
R162 = NC	R162 = NC
C105 = NC	C105 = NC
C30 = NC	C30 = 10PF
L11 = NC	L11 = 220NH
C94 = NC	C94 = 220PF
R295 = 75 1%	R295 = 0
C319 = NC	C319 = NC
C61 = NC	C61 = NC
C2 = 1UF	C2 = NC
U2 = FMS6141	U2 = NC



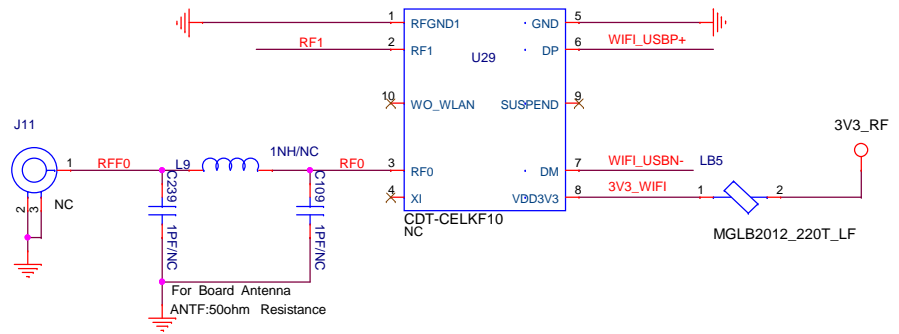
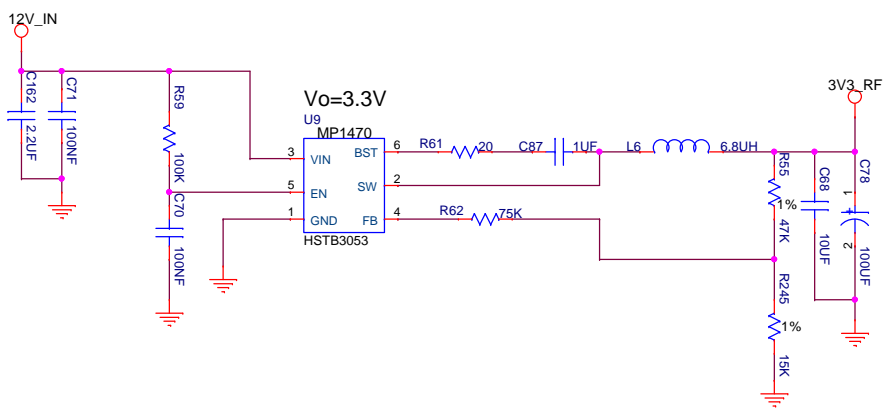
**\*\* Design guideline \*\***

- 1.All channel traces should be separated from other traces by GND.
- 2.ESD components are suggested for ports protection, default BAV99.

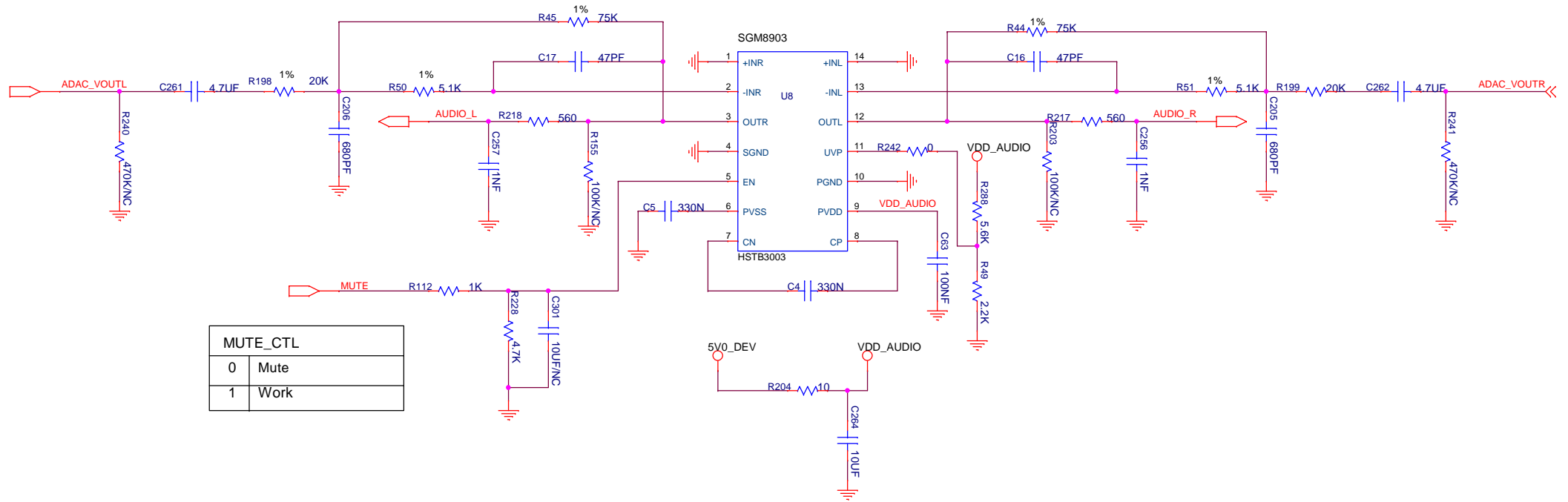
# USB WIFI



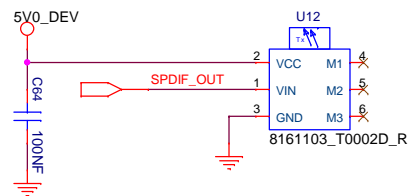
# POWER OF WIFI



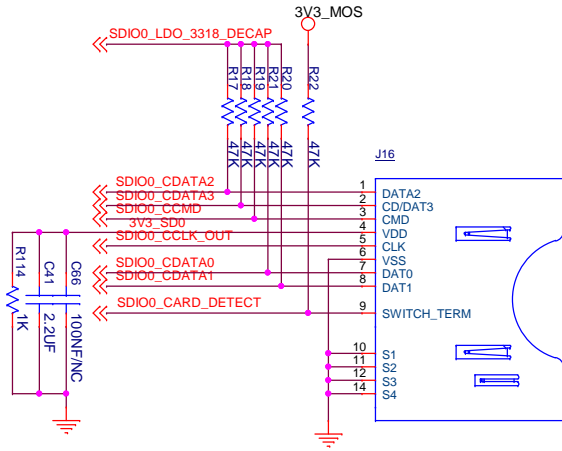
# AUDIO OUTPUT



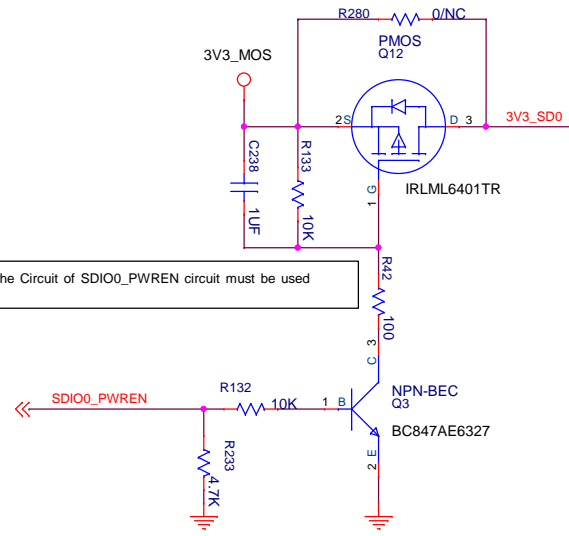
# SPDIF



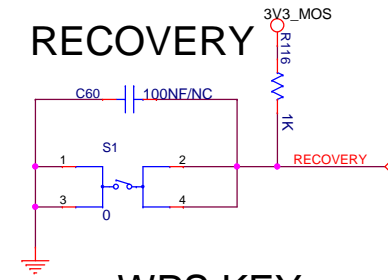
# SD CARD/IR/LED/KEY



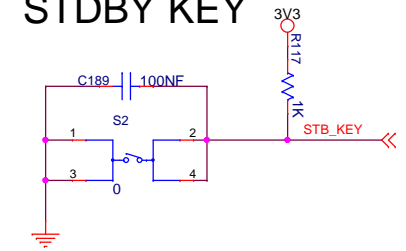
IF support SD3.0 the Circuit of SDIO0\_PWREN circuit must be used



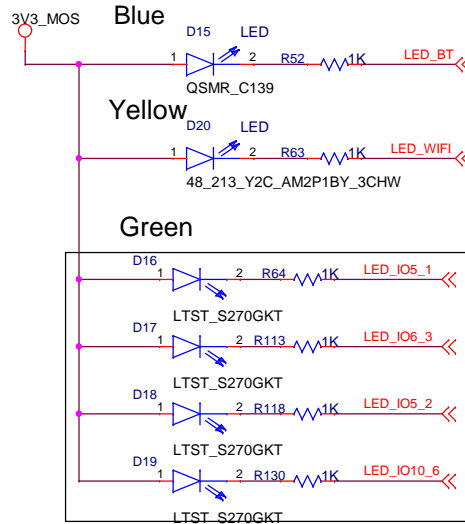
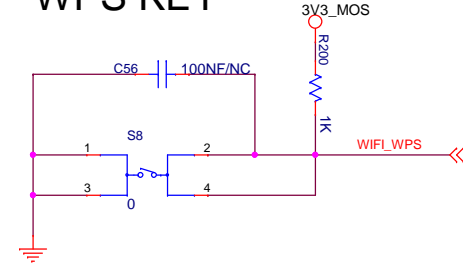
## RECOVERY



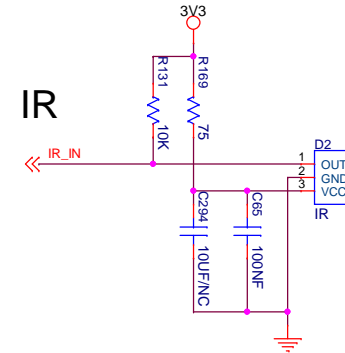
## STDBY KEY



## WPS KEY

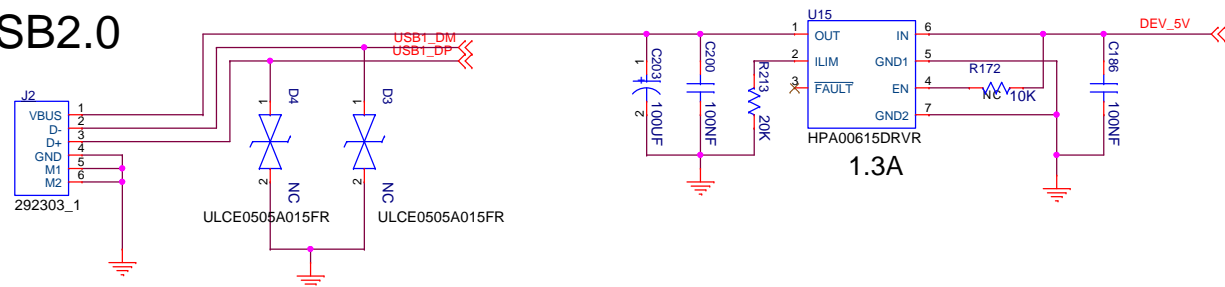


## IR

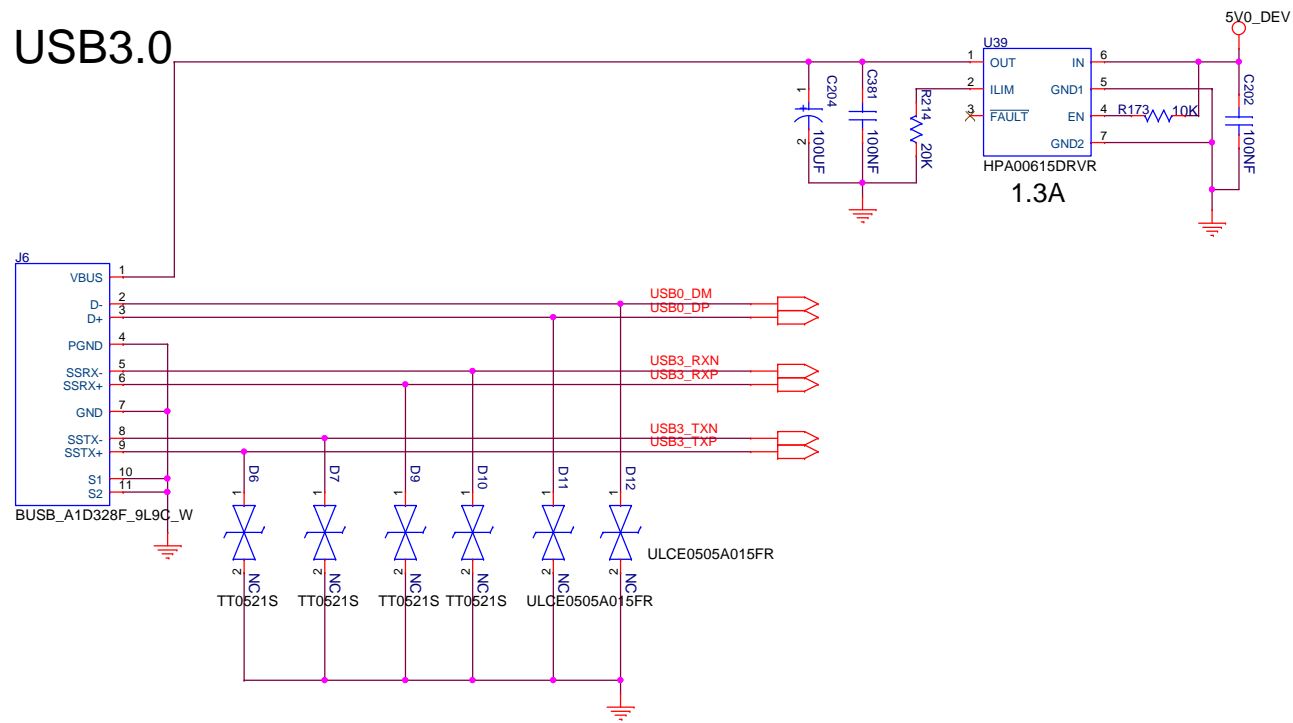


# USB2.0 & USB3.0

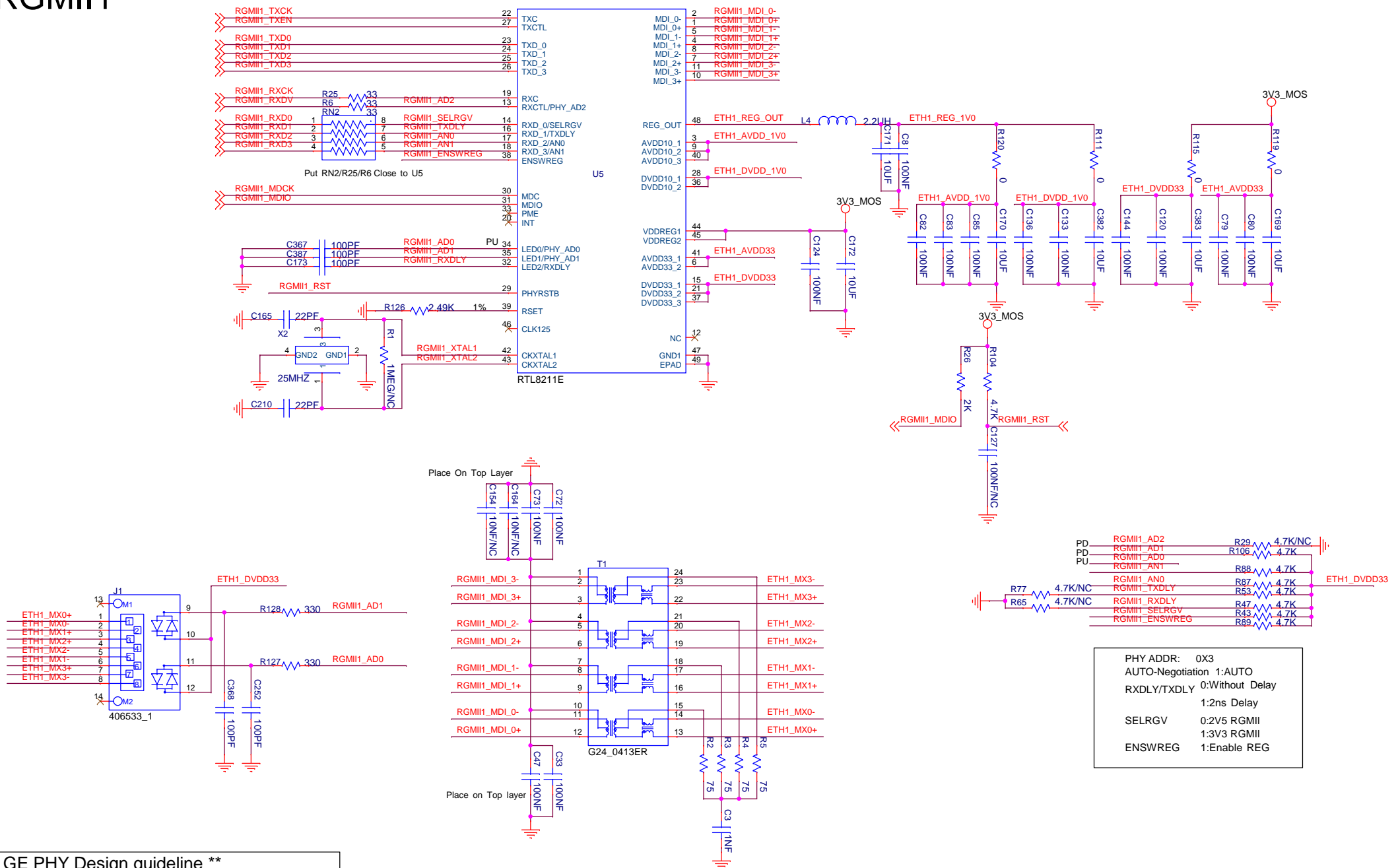
## USB2.0



## USB3.0



# RGMII1

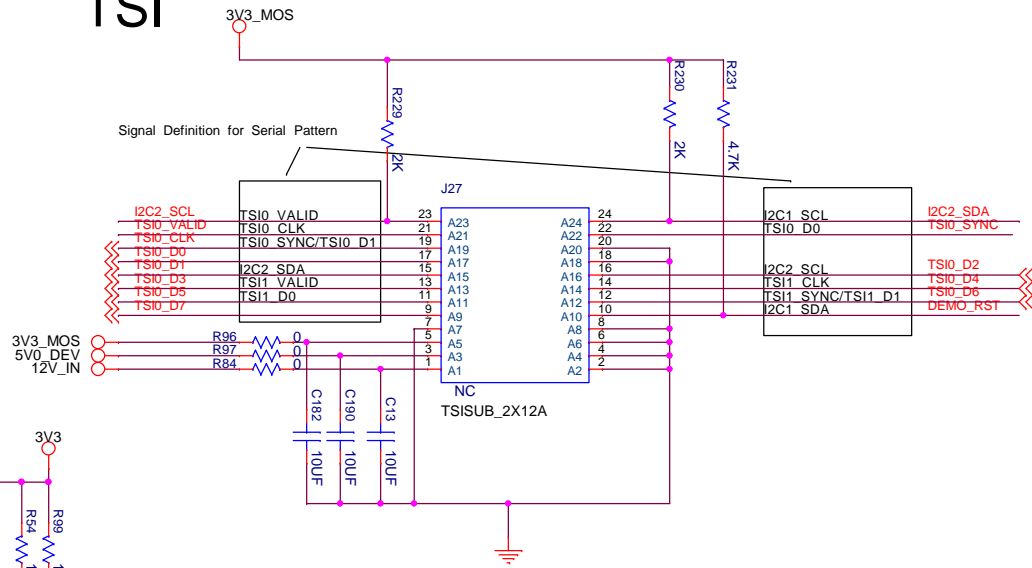


**\*\* GE PHY Design guideline \*\***

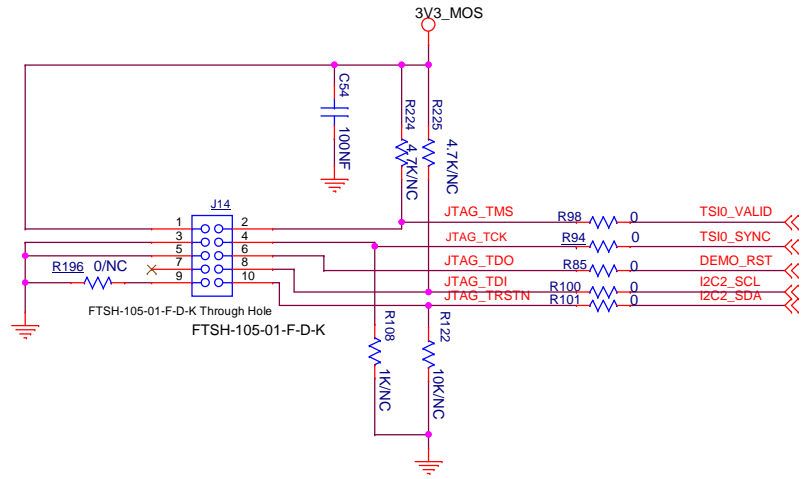
A.RGMII interface

- 1.The TXCK and RXCK trace should be separated from other traces by GND.
- 2.The Power layout of GE PHY should copy Hisilicon demo completely.
- 3.The RXD[3:0] and TXD[3:0] should be separated from other traces by GND.

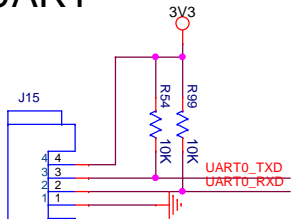
# TSI



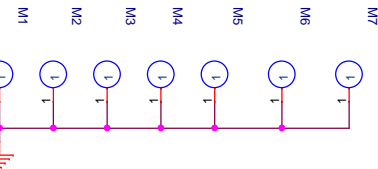
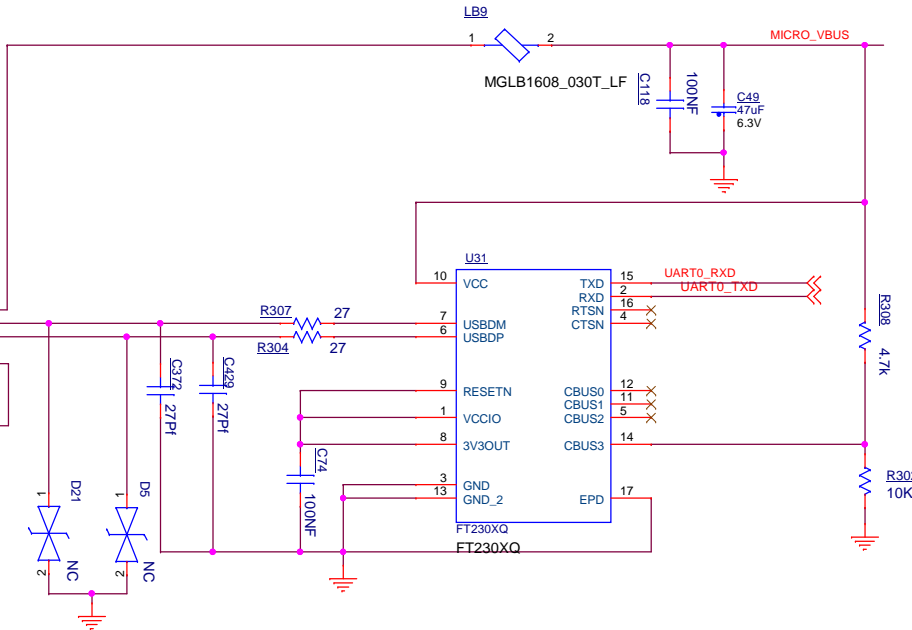
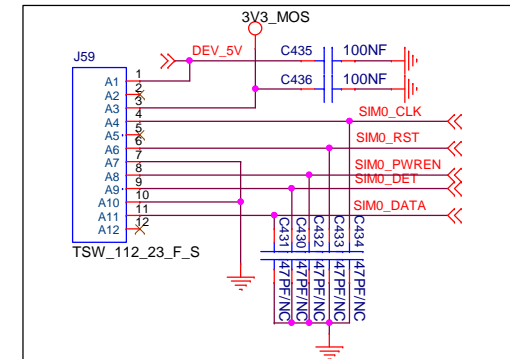
# JTAG



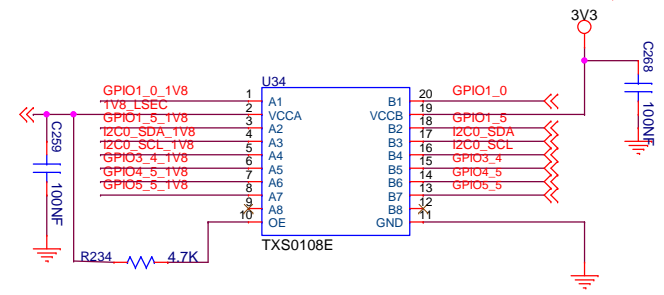
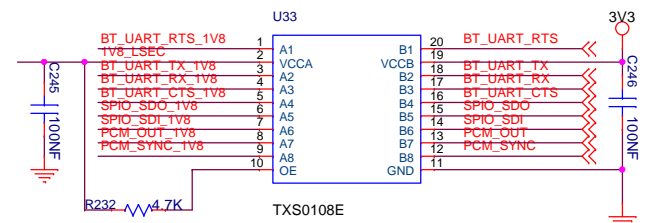
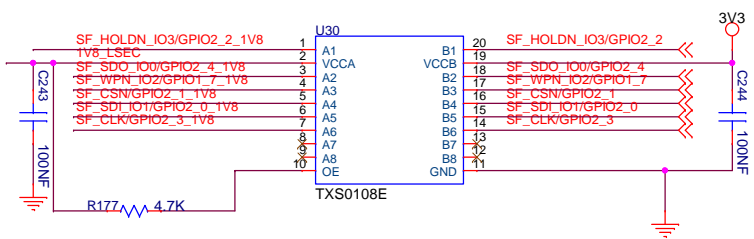
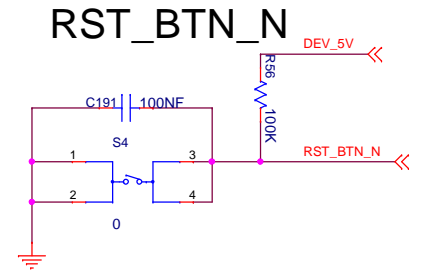
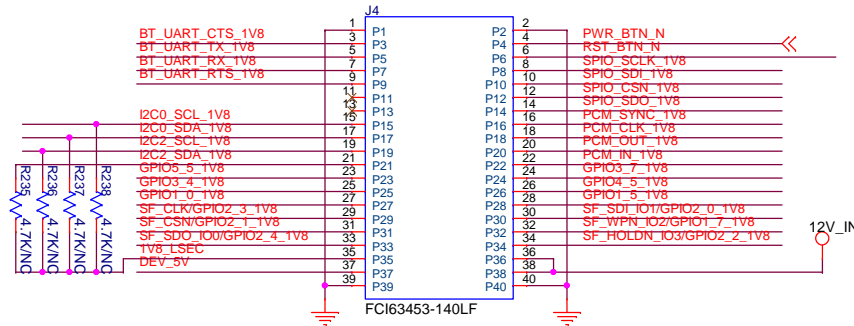
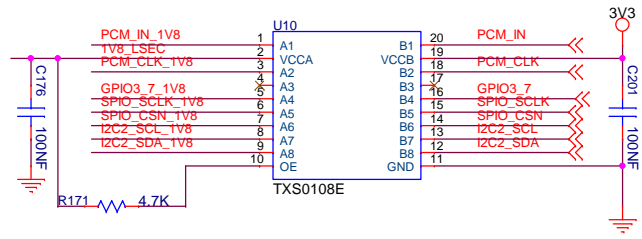
# UART



# Connector for Smart Card Board

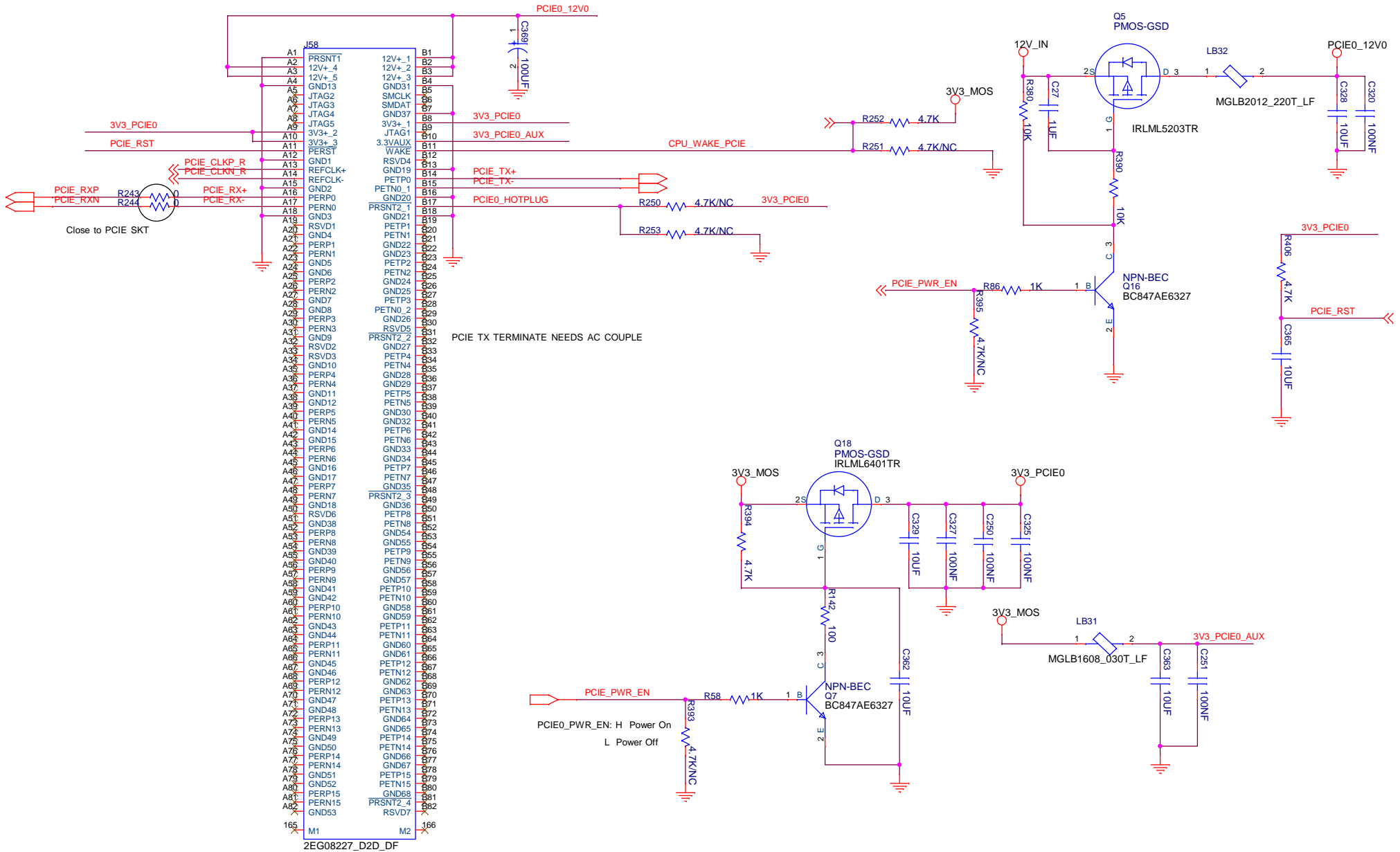


# Low Speed Expansion Connector(LSEC)





# PCIe 1 lane



PCIe\_Socket

Schematic Update Record

Version	Date	Author	Change Note	Note
V0.1	20160308	HEMINGXIAO	The 1st Version	
V0.2	20170828	HEMINGXIAO ZhangBingFeng	1. Add R299=1K and D24 Red LED indicator. 2. Add R125=47K and R141= 47K pull up resister. 3. Change J14 from 8 Pin connector to 10 Pin connector . 4. Change power supply of USB to UART circuits.	
V0.3	20180311	ZhangJiaYue	1.Update the version to VER.B. 2.Add R407=0ohm to connect GPIO3_5 for WIFI_RST. 3. Remove DTV turner board and smrart card ciruits.	